IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

#13/B

In re TRADEMARK Application of:

Haruko INOUE et al.

Serial No.: 09/666,156

Filing Date: September 19, 2000

Title: HIGH-VOLTAGE MOS TRANSISTOR AND METHOD FOR FABRICATING THE SAME

Group Art Unit: 2811

3/19/03

Examiner: Loke, Steven Ho Yin

John H

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as First Class Mail in an envelope addressed to: Commissioner for Patents, Washington, D.C. 20231, on February 27, 2003.

April Campbell

April Campbell

AMENDMENT UNDER 37 C.F.R. 1.116

BOX AF
Commissioner for Patents
Washington, D.C. 20231

Sir:

The following is presented in response to the Office Action mailed December 3, 2002, in connection with the above-captioned patent application.

IN THE CLAIMS:

Please cancel claims 1-4 and 7.

Please amend claim 5 as follows:

SUB C2 fig. 4 B1

5. (Twice Amended) A high-voltage MOS transistor wherein a dopant concentration of a source offset region is set lower than a dopant concentration of a drain offset region and thereby a resistance value of the source region is set independently of a resistance value of the drain region in such a manner as to maintain a high sustaining breakdown voltage of the high-voltage MOS transistor, which is based on a voltage of the source offset region and a voltage of a substrate region directly under a gate insulating film during operation of the high-voltage MOS transistor.